

#### CA-SpaceNet: Counterfactual Analysis for 6D Pose Estimation in Space

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> Code: <u>https://github.com/Shunli-Wang/CA-SpaceNet</u> Video: <u>https://www.youtube.com/watch?v=h-vzCdersVQ</u>



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- 1. Background & Motivations
- 2. Proposed CA-SpaceNet
- 3. Experimental Results
- 4. Conclusion



#### I. Background & Motivations

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#### **1. Background & Motivations**



Basic technology

Reliable and stable 6D pose estimation algorithms



SpaceX Crew-2 Docking Mission



Preview of the ClearSpace-1

Challenges in the space scene:



Harsh imaging conditions



Background interference



Limited power consumption



### 1. Background & Motivations



Quantization inference and the PIM accelerator architecture.



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Basic components of a two-stage 6D pose estimator.

Actual network structure (CA-SpaceNet)

Factual path: Extract the feature of the whole image.

**Counterfactual Path:** Extract the feature of the background information.

**Pseudo Counterfactual Path:** Mimic the output feature of the counterfactual path.











> Training: FPN<sub>pc</sub> will imitate FPN<sub>c</sub> by maximizing the similarity between  $\{\mathbf{F}_{n}^{pc}\}_{n=1}^{N}$  and  $\{\mathbf{F}_{n}^{c}\}_{n=1}^{N}$ . Total Loss:  $\mathcal{L} = \lambda_{3D}\mathcal{L}_{3D} + \lambda_{c}\mathcal{L}_{cls} + \lambda_{s}\mathcal{L}_{sim}$ 

> **Testing**: the whole counterfactual path will be removed during inference.







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# TABLE ICOMPARISON WITH STATE-OF-THE-ARTS ON SWISSCUBE.MethodNear $\uparrow$ Medium $\uparrow$ Far $\uparrow$ All $\uparrow$

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SegDriven [39]	41.1	22.9	7.1	21.8
SegDriven-Z [39]	52.6	45.4	29.4	43.2
DLR [5]	63.8	47.8	28.9	46.8
WDR [4]	65.2	48.7	31.9	47.9
WDR* [4]	92.37	84.16	61.27	78.78
CA-SpaceNet	91.01	86.32	61.72	79.39

TABLE III Comparison with State-of-the-arts on SPEED

Method	$\mathbf{e}_q + \mathbf{e}_t \downarrow$
SLAB Baseline [3]	0.0626
pedro-fairspace [42]	0.0571
WDR [4]	0.0180
WDR* [4]	0.0400
CA-SpaceNet	0.0385

#### TABLE II

Comparisons of the re-training WDR\* model and the CA-SpaceNet.

Method	Near ↑	Medium ↑	Far ↑	All ↑
WDR* [4]	92.37	84.16	61.27	78.78
WDR* [4] w. 30-Ep.	89.93 (-2.44)	82.09 (-2.07)	56.50 (-4.77)	75.76 (-3.02)
CA-SpaceNet	91.01 (-1.36)	<b>86.32</b> (+2.16)	<b>61.72</b> (+0.45)	<b>79.39</b> (+0.61)

- The CA-SpaceNet can eliminate the interference of background through counterfactual analysis under the *Medium* and *Far* setting.
- The performance improvement is brought by the counterfactual analysis strategy rather than the additional 30 training epochs.

WDR\*: note that the results of WDR on SPEED is obtained by the original paper without source code. We reproduced this model and reported our results as WDR\*.





However, with the help of the causal inference strategy, the CA-SpaceNet successfully handles these complex situations. The CA strategy is able to weaken the adverse impact of background interference to the final results.

**Results of** 

**CA-SpaceNet** 

**Results of** 

WDR\*



TABLE IV

RESULTS ON THREE DIFFERENT QUANTIZATION MODES OF 8-BIT AND 3-BIT CA-SPACENET ON SWISSCUBE

#Bits	Quan. Mode	ADI-0.1d ↑	OPs & FLOPs	Perc.(%)
	Ι	76.21	36.91 GOPs + 33.79 GFLOPs	52.21
8	Π	75.04	44.51 GOPs + 26.19 GFLOPs	62.96
	III	74.65	70.47 GOPs + 0.23 GFLOPs	99.67
	Ι	75.10	36.91 GOPs + 33.79 GFLOPs	52.21
3	Π	74.47	44.51 GOPs + 26.19 GFLOPs	62.96
	III	68.68	70.47 GOPs + 0.23 GFLOPs	99.67

#### TABLE V

SUMMARY OF PARAMETER STORAGE SIZE

Format	#Para.	Model Size	Stor. Saving (%) $\uparrow$
FP32	51.29 M	205.17 MB	0.00
8-bit	51.29 M	51.29 MB	75.00
3-bit	51.29 M	19.23 MB	90.63

#### TABLE VI

MEASURED LATENCY ON DIFFERENT HARDWARE

Device	Latency (ms) $\downarrow$
ARM v8.2 64-bit CPU (Nvidia Xavier) Intel Core i7-8700K CPU	26.16 10.25
PIM Arch. on Ultra96v2 FPGA	5.99

> The quantization can <u>save a large mount of GFLOPs</u> without significantly reducing the performance.

- > Quantization greatly reduce the size of the network which makes the model easier to be deployed on devices.
- > Latency test results of the PIM chip shows the high efficiency of the quantization and our actual deployment.





and 1.7x speedup compared with Intel Core i7-8700K CPU.



Our real deployment of the **PIM architecture** on the Ultra96v2 FPGA achieves:

4.4x speedup than ARM v8.2 CPU, &
1.7x speedup than Intel Core i7-8700K CPU.



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#### 4. Conclusion



- We propose a framework named CA-SpaceNet, which is robust to the interference of complicated background information.
- Our approach outperforms state-of-the-arts on the challenging SwissCube dataset and achieves competitive results on the SPEED dataset.
- We quantize the CA-SpaceNet into a low-bit-width model and deploy a part of the quantized network into a Processing-In-Memory (PIM) chip on FPGA. Low latency proves the feasibility of our method.





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